Analog BIST for ADCs – A modern case study

Summary

Built-in self-test has long been hailed as the solution to increased analog test costs and increasingly difficult access into SoCs. ATEEDA's LinBIST recently received additional validation by STMicroelectronics as a BIST alternative to high capital cost conventional analog test equipment. A 50MHz, 12-bit ADC in 55nm CMOS process was fabricated incorporating LinBIST's test structures. The results were found to match or exceed the performance of the conventional test approach, and full characterisation was also achieved using only digital connections to the device.

Introduction

A reputation for delivering in-specification parts is vital to any System on Chip (SoC) manufacturer. However, it can be lost in an instant when inadequately tested parts slip through the net. Test is no place to cut corners but high quality comes at a price. The industry norm for test now exceeds 20% of production costs and can now exceed wafer cost. Moore's law shrank digital transistors but the die size remained about the same. That can mean hundreds of millions of gates to test on each die. Digital testing has admirably risen to the challenge and highly compressed digital tests have kept ahead of the growth in circuit complexity to control costs. The same cannot yet be said for the analog circuitry in SoCs. More functionality is crowded on to the die but physical access has barely increased and analog test equipment struggles to match the growth in complexity and need for parallelism. The analog circuitry can be small compared to the huge digital blocks on an SoC, but factors like the high capital equipment cost, long test time, length of test development and verification, all make the analog test costs dominant.

Analog built-in self-test (BIST) has a history of groundbreaking approaches sometimes even making commercial products, only to disappear before gaining traction. Being too early is as bad as being too late. For analog BIST neither the market nor the semiconductor process nodes were ready. Other ways to cut costs had still to be exploited: more capable testers especially using more parallelisation; more off-shoring of test function etc, even custom in-house BIST and DFT solutions. Ten years ago the brick wall limiting SoC test cost reduction had not loomed so large and the prevailing process nodes made BIST uneconomic. That generation of entrepreneurial BIST companies had ambition but lacked resources to deliver commercially.

Things are different now in several important ways. After several Moore's law cycles 1M gates per square millimetre gives ample cheap digital raw materials. Smart algorithms are still needed, but with ingenuity and avoiding extravagant design, synthesis on-chip is now fairly cheap. The inexorable drive from Analog to Digital domain for ever more functions makes an analog BIST strategy for DACs and ADCs cover a lot of ground. A small number of other analog circuits must be on the roadmap (PLLs and SerDes,) but focus is the key to building traction.

This paper describes how the largest most successful SoC companies benefit by embracing innovations in analog test. A case study of a BIST strategy validation program by Europe's leading Integrated Device Manufacturer, STMicroelectronics is presented. The size of investments involved in SoC development nowadays demand the highest levels of proof and rigour in validation before adopting any changes. Quality is paramount and changes must deliver improved performance irrespective of cost or time savings.

Any shift from the conventional use of analog or mixed signal testers to BIST to allow use of simper digital testers must be thoroughly validated. Only then can it be introduced into production devices or centralised IP libraries. The largest companies often run Multi Project Wafers (MPWs) to check out performance characteristics of new designs and process partly for this purpose.

Analog BIST

ATEEDA offers LinBIST as the world's first pushbutton tool for analog BIST. Initially focussing entirely on converters, the EDA tool allows users rapidly to customise digital IP (embodied as Verilog) working in synergy with proprietary reference analog IP. Together these give a small, completely autonomous BIST block, able to be integrated with the circuit under test. No Verilog needs to be written manually because the GUI automates the process. It enables selection of the target ADC specification, entry of the test limits, the type of interface required and finally outputs the Verilog for synthesis. The analog IP is designed to have limited requirements for customisation to any customer target IP.

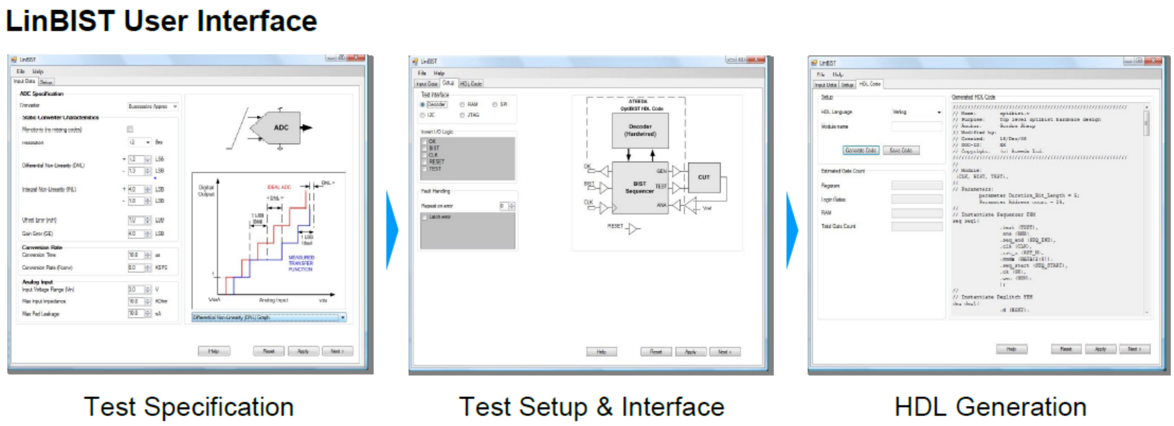

Figure 1 LinBIST GUI screenshots and use

Figure 2 shows the tool flow for using LinBIST with the customer's standard tool flow to produce the completed design ready for synthesis and verification:

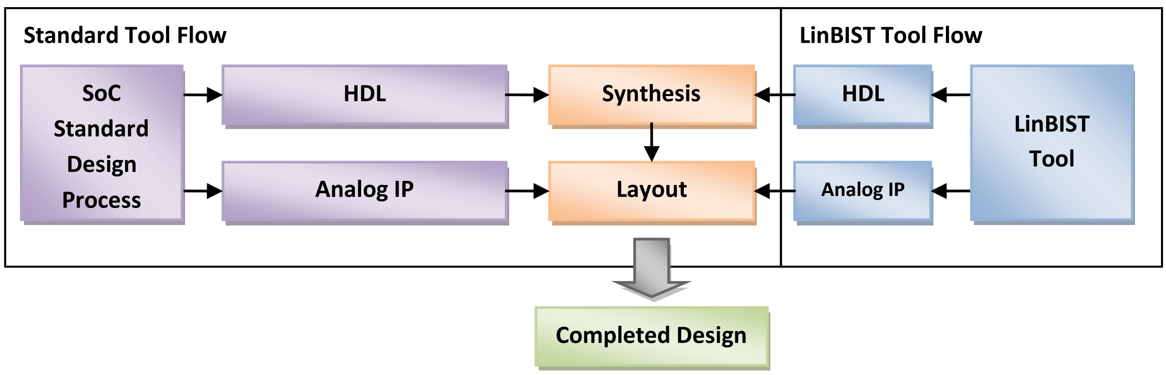

Figure 2 LinBIST integration with standard Design tool flow

Normally at this point the completed design consisting of the ADC with the LinBIST IP would proceed directly to synthesis and be the subject of the customer's standard verification process. ST however, took the opportunity to add some additional validation features.

LinBIST validation for STMicroelectronics Production Process and Devices

ATEEDA already had functioning LinBIST 0.18u CMOS silicon and an extensive suite of simulation-based verification steps had been run before releasing the product externally. These included running dozens of scenarios with hundreds of thousands of test cases. These proved the effectiveness of the IP even in the presence of significant levels of noise, wide-tolerances, temperature variations and limited on-chip component matching.

ST executed its own validation program to ensure the BIST delivered the highest standards of quality and effectiveness. It was decided to make silicon incorporating LinBIST on-chip to test one of ST's Library 55nm CMOS process 12-bit, 50MHz ADCs. Additional structures to validate the performance were also included on the chip. It is important to note these additional steps would not necessarily be required for other customers for BIST adoption as it is now silicon-proven at different nodes.

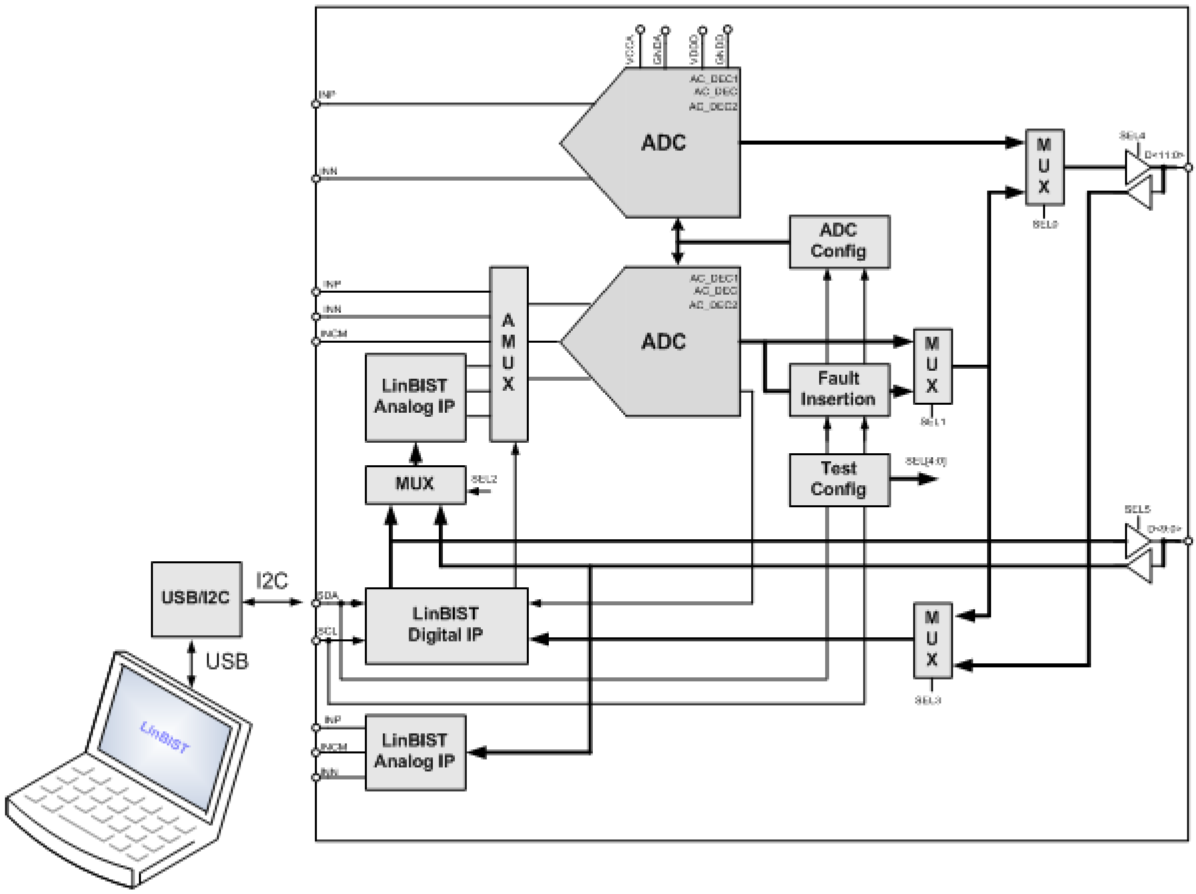

Figure 3 Test chip structure

The extra structures permitted a variety of faults to be programmed digitally into LinBIST's array of built-in registers via an I2C interface on the chip as shown in Figure 3. These ranged from simple offset or gain errors through to fractional DNL or subtle INL errors affecting distortion and ENOB.

The completed design of the validation chip proceeded to synthesis and verification where full mixed signal simulations were run on Mentor Graphics Questa® ADMS mixed signal verification environment by exporting it from the original Cadence® Netlist. Full transistor level and Verilog VHDL AMS simulations ran in less than 30 minutes showing the system to be fully operational including the extra structures and the communications ports which permit external setting up from a tester or a laptop. ST then applied their normal verification procedure and the chips were fabricated and packaged for test.

Testing the Working Silicon

The performance of the silicon including the ADC and the BIST was independently tested by both ATEEDA and ST. ST designed a tester load board to verify performance against existing approaches using Mixed Signal Tester with a converter test option (CTO).

In addition ATEEDA created a simple test PCB with sockets for the chip (Figure 4) and USB interfaces to communicate with the BIST's own I2C interface.

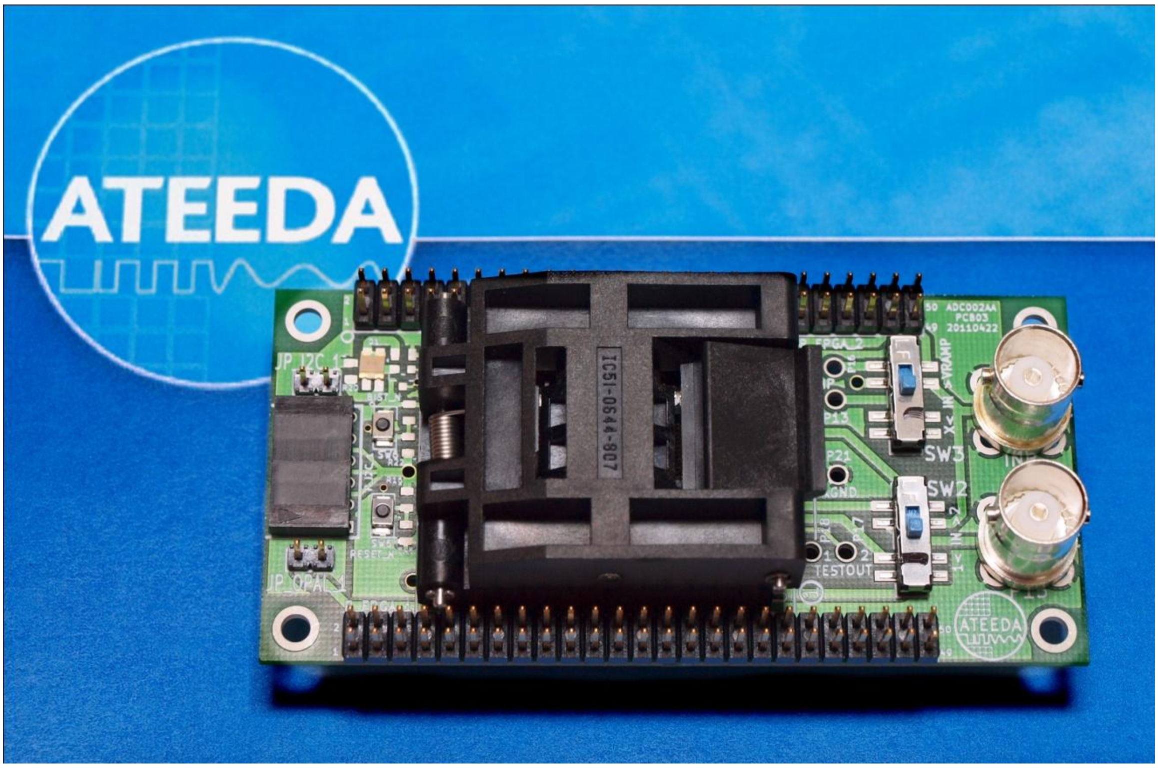

Figure 4 LinBIST chip USB-based test and characterisation socketed board

Individual tests could be selected for execution from a laptop. The results showed that on all the metrics, the BIST performance equalled or exceeded that of the conventional test. In addition the BIST was sufficiently sensitive that in addition to binary pass/fail decisions it could be used for characterisation purposes. LinBIST incorporates a characterisation option which can identify arbitrary limits of any of the tested parameters. It works by repeating many tests to make very precise measurement of the pass/fail threshold. Such characterisation is simpler (especially for example in an oven for temperature cycling) than conventional approaches since only digital signals need be communicated.   The 55nm packaged silicon was subsequently tested and characterised internally by ST and separately using LinBIST's characterisation software as seen in Figure 5.   LinBIST has a GUI which can communicate directly with the on-chip IP through its USB port to the I2C interface.

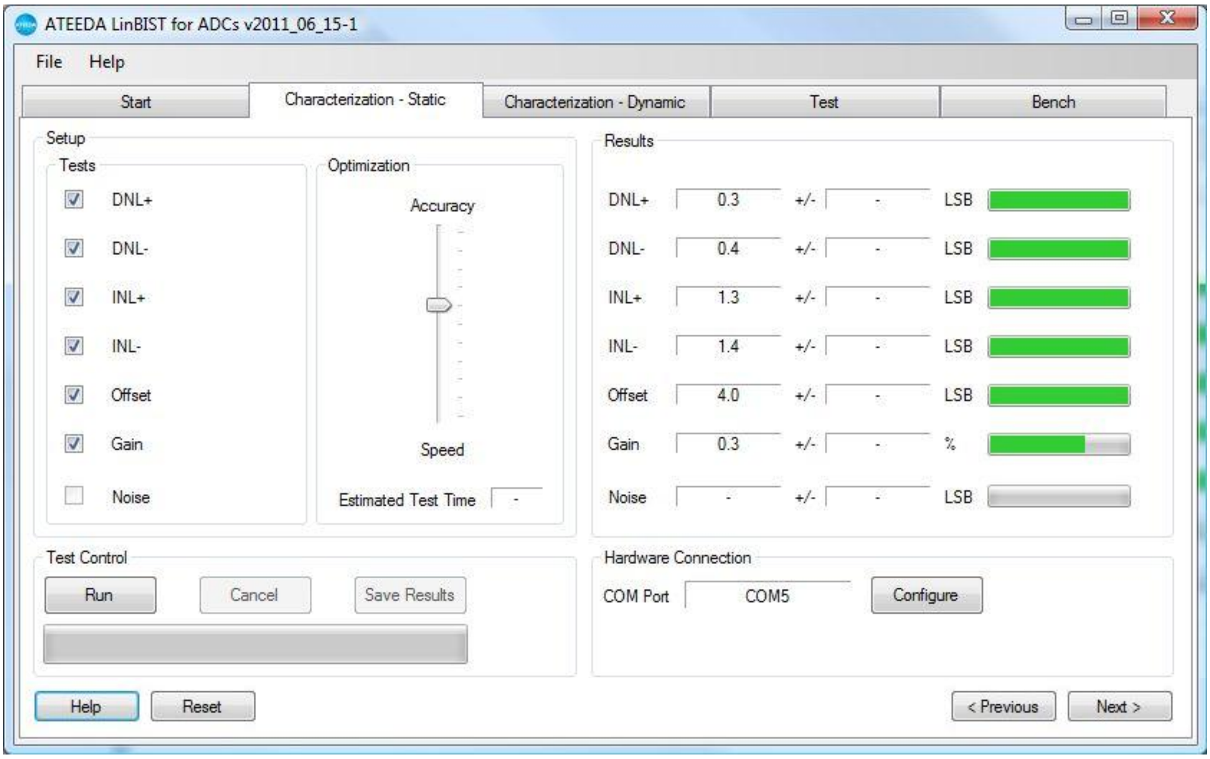

Figure 5 LinBIST's ADC characterisation tool

Results, Conclusions and New Developments

Although the technical details of the tests are confidential, they confirmed that the performance matched or exceeded the conventional production test results. Having the tests on-chip allows faster tests to be carried out due to the intrinsically lower noise or alternatively permits tighter specs to be tested in a shorter time. The density of transistors on advanced nodes permits economic use of high quality BIST giving a performance that matches or exceeds conventional external test equipment with intrinsic advantages.   Cost reductions and improved access to crowded SoCs offer a compelling incentive to adopt innovative test solutions and LinBIST makes the process straightforward for designers to embrace.

ATEEDA offers comprehensive converter BIST capabilities that covers ADCs ranging from sensors, high quality audio and video across the gamut of tested parameters from static DNL, INL etc and recently added dynamic metrics, THD and SFDR. Fully on-chip DSP gives autonomous tests exploiting intrinsic noise immunity and robustness while flexible interfaces make set up and characterisation straightforward.

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